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The study on un-doped/boron doped/un-doped triple SEG in vertical NAND flash memory

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Abstract

Selective epitaxial growth (SEG) plays a critical role in vertical NAND flash memory because it serves as a ground select line (GSL) transistor, which is used to control the cell current in the vertical channel. In this study, different channel hole sizes between the adjacent hole and away hole from the common source line (CSL) were detected after vertical channel etch (VCE). This discrepancy severely impacts the boron concentration of SEG applied through *ex-situ* boron implantation, and results in large GSL Vth variations. Novel *in-situ* boron-doping of triple-layered un-doped/boron doped/un-doped SEG was developed to solve the high variation of the boron concentration in SEG caused by different channel hole sizes. A series of experiments was designed and performed to determine the optimal height and concentration of the boron doped SEG. Finally, the optimized boron-doped SEG in the triple-layer SEG was shown to improve the distribution of the GSL Vth without deterioration of the SEG height uniformity.

1. Introduction

The scale of NAND flash memory in the market is rapidly increasing, caused by the high demand for smartphones, desktop PCs, and solid-state disk drives. The continuous enhancement of NAND flash memory storage capacity is necessary because of the increasing storage requirements of applications. The storage capacity is determined by the number of devices in a chip, called the degree of integration. To increase the bit density in each space, the feature size and the distance between cells should be reduced. Based on the ITRS flash roadmap, the half-pitch of two-dimensional flash memory is 18 nm in 2013. [1] However, the additional shrinkage of feature size and distance between cells causes problems related to physical, electrical, and reliability limitations. The physical limitations create unwanted diffraction and scattering during the lithography process due to the line width of the device features being slimmer than the laser wavelength.

One of the electrical limitations is electric field crowding, caused by the small size of the floating gate. The others are cell to cell interference, hot carrier distribution, and channel boosting potential due to short cell to cell distances. When the size of a floating gate is greatly reduced, the number of electrons that can be stored is also significantly reduced. Therefore, if electron loss occurs, the cell information can be changed. Many researchers have investigated both increasing the degree of integration and solutions for scaling limitations. As a solution, the vertical structure has been proposed, which stacks cells in a vertical array instead of shrinking the feature size. This form has been used with the two-dimensional planar NAND flash memory technology since 2013.

Toshiba announced pipe-shaped BiCS (P-BiCS), [2] which is an upgraded type of BiCS. The P-BiCS uses a U-shaped folded channel to avoid thermal damage to the select transistors during the BiCS fabrication process. At the same time, Samsung announced their vertical memory architecture, the Terabit Cell Array Transistor (TCAT), shown in the schematic. It possesses a reduced cell size compared to BiCS, which was achieved by different improvements to the process technology. The TCAT adopts a metal (tungsten) gate structure that leads to a faster operation speed and better reliability compared to those of BiCS. However, both the P-BiCS and TCAT adopt the "punch and plug" process for vertical channel formation. The TCAT went into mass production in 2020 [3].

Numerous epitaxial growth techniques have been researched thus far. The representative epitaxial growth techniques are liquid-phase epitaxy (LPE), solid-phase epitaxy (SPE), and vapor-phase epitaxy (VPE). The characteristics of these techniques are summarized in Figure 1. The well-known Czochralski method, used to grow wafer ingots, is one conventional form of LPE. Recently, LPE using a laser was reported by Son *et al.* for application to semiconductor devices. Son *et al.* used a Nd:YAG laser with a wavelength of 532 nm to form epitaxial layers for three-dimensional devices. The authors named the method laser-induced epitaxial growth (LEG). However, this method cannot be used on devices, because of a high thermal budget that generates leakage. VPE of silicon is one the most common methods to grow epitaxial layers on silicon substrates in modern VLSI devices.

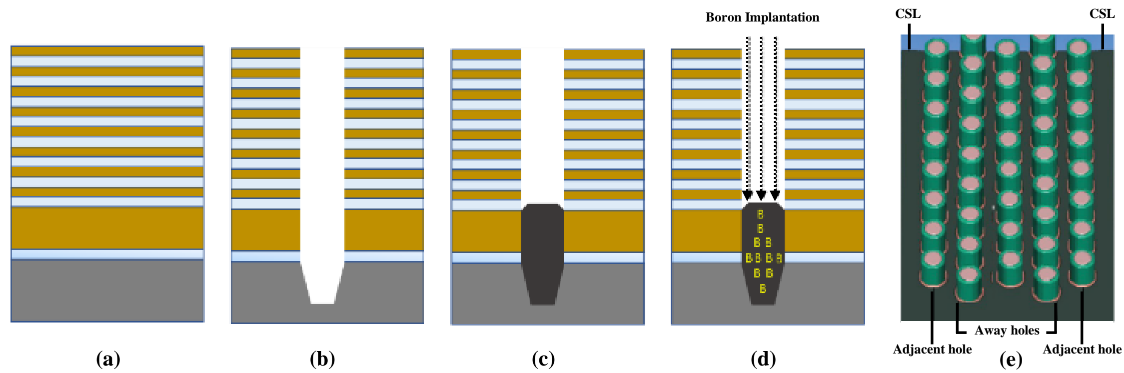


Figure 1. The illustration from VCE to SEG Implantation. (a) Alternating silicon oxide layer and silicon nitride layers deposition on silicon substrate (b) After VCE (c) After SEG (d) After Boron Implantation (e) Top view of VCE.

Currently, selective epitaxial growth (SEG) is being intensively studied as a performance booster for advanced CMOS technologies. Epitaxial silicon and silicon alloys such as SiGe, SiC, and SiGeC are selectively grown using VPE processes. Using an elevated source/drain is known to reduce contact resistance of source/drain regions and can suppress short channel effects. Embedded silicon alloys are recognized as beneficial to strain engineering for the mobility enhancement of channel regions. The term, "selective" means that epitaxial layers are grown only on the exposed silicon surface, not on SiO_2 or Si_3N_4, which permits the reduction of photolithography and etching processes. Since VPE requires relatively high temperatures for chemical reactions, it is unavoidable that silicon or its alloys form stable polycrystalline clusters on oxide and nitride layers as well as epitaxial layers on exposed single crystalline seeds. The SEG method uses etching chemicals such as HCl and Cl_2 during VPE processes to make volatile phases of silicon and its alloys and finally to remove nucleation sites on oxide and nitride films. It is crucial to eradicate these nuclei on oxide and nitride layers before they cause agglomeration and form stable clusters, which cannot be etched away during SEG processes (e.g., selectivity loss). Since the growth and etching of silicon occur simultaneously and reversibly, the precise control of SEG process conditions is required to obtain a selectivity window, beyond which selectivity loss or etching of the single crystalline seed is observed.

The SEG process plays an important role in vertical NAND flash memory because the SEG area functions as a ground select line (GSL) transistor, which is used to properly control the cell current variation caused by the changes in channel length between the adjacent hole and away hole from the common source line (CSL). However, boron implantation after SEG could result in an uneven boron concentration in the SEG area owing to the channel hole size and SEG height variations. This severely impacts the GSL Vth distribution, resulting in a decreased operating margin. The minimum cell array element of vertical NAND flash memory is from the SSL to the GSL, which is defined as string. When programming, GSL is applied as ground, but if GSL Vth distribution deteriorates, the program distribution deteriorates. Additionally, the uniformity of the SEG height is crucial to the GSL leakage current since an improperly thick SEG is close to upper wordlines and leads to insufficient physical isolation. As a result, it could induce shorts between the GSL and upper gates. The vertical channel etch (VCE) of vertical NAND flash memory is usually a high-aspect-ratio hole structure etched into a Si wafer, through alternating silicon oxide layers and silicon nitride layers (Figure 1). Unfortunately, the channel hole size and shape change between the adjacent hole and away hole from the CSL, because of the etch loading effect. [4] This effect changes the boron transfer efficiency to the SEG during boron implantation and causes an impurity difference at the Si interface from hole to hole, resulting in deterioration of the SEG height distribution. Ion implantation is a low-temperature process by which ions of an element are accelerated into a solid target. In this case, the ion implantation amount reaching the bottom SEG is varied according to the CD and bending of the channel hole. During the pre-cleaning process before SEG, the plasma methods used also change the efficiency of etchants reaching the bottom sub-silicon surface according to the channel hole profile, which leads to incomplete impurity removal, which increases the SEG crystal defects and affects the growth rate. However, when the conditions are altered to increase the etching of the sub-silicon surface, hole-to-hole bursting occurs through the change of the top of the channel hole. In response, several methods for removing impurities at the Si interface have been designed. [5] Halogen-containing plasma etch treatments (PETs) have been developed to remove the damaged layer and impuritie. For these treatments ClF is formed in Cl-based PETs and HF is formed in HBr-based PETs; both HF and Br atoms have relatively low silicon nitride etch ability, and they do not induce nitride damage. However, no implantation method overcoming the problems induced by the shape of the channel hole profile has yet been reported. To solve this, there is a barrier to overcome: the difference in channel hole profile between the adjacent hole and away hole from the CSL with increasing mold height. In this work, *in-situ* boron-doping of SEG was studied for comparison with boron implantation after un-doped SEG. A triple-layered structure of un-doped/boron-doped/un-doped SEG was proposed to solve the non-uniform transfer of boron, to improve the Vth distribution of GSL transistors. The development of the triple-layer SEG was essential, because the boron-doped SEG became uneven on the sub-silicon layer, owing to the rapid growth rate induced by the boron. This growth rate increase was caused by an enhanced H-desorption when B atoms are present on the surface, freeing surface sites for the adsorption of Si gaseous precursors. [6] Accordingly, it was confirmed that the use of boron doped SEG in the region for operating the GSL transistor improved the GSL transistor Vth distribution without deteriorating the SEG height variation.

2. Experimental details

The wafers used in this study were prepared by alternating the deposition of silicon oxide and silicon nitride. Silicon oxide is normal used 200~300Å and silicon nitride is normal used 300~400 Å.

An amorphous carbon hard mask was deposited on the top layer and patterned by lithography and plasma etching. The residual hard mask was subsequently removed by O_2 ashing and wet cleaning. VCE is a plasma etching method, it etches silicon oxide and silicon nitride at once.

Figure 2(a) shows the process schematic of the clearance before SEG and the *ex-situ* boron implantation after SEG. SEG was performed with a rapid process system in a single chamber. The gases used were DCS, HCl, and H_2, the temperature was above 800°C, and the pressure was below 100 Torr. SEG is deposited only on silicon of the bottom hole while co-flowing DCS and HCl. HCl suppress silicon adsorption on silicon oxide and silicon nitride of the mold. The SEG height is 800~1200 Å based on sub silicon.

Boron implanting was carried out in a beam implantation chamber. The ion energy is 30~40 KeV. Figure 2(b) shows the process schematic involving the *in-situ* boron doping SEG process, which was performed in the same chamber with B_2H_6. In doped SEG case, undoped SEG and doped SEG are performed *in-situ*. Undoped SEG is co-flowed DCS and HCl, and doped SEG is co-flowed DCS, HCl, and B_2H_6 together.

All analysis was performed on patterned wafers, the boron profile was inspected by secondary ion mass spectrometry (SIMS), and the SEG height was measured from transmission electron microscopy imagery.

3. Results and discussion

3.1 Analysis of the distribution of boron and GSL Vth

The boron profile of the SEG was analyzed after *ex-situ* boron ion implantation on channel hole patterning wafers by SIMS. As shown in Figure 3(a), the boron concentration of the away hole is lower than that of the adjacent hole. Because the away hole has a smaller hole size and severe bending compared to the adjacent hole, the boron ion efficiency reaching the SEG decreased. In contrast, the *in-situ* boron-doped SEG exhibits a boron profile that is uniform between the adjacent hole and the away hole (Figure 3(b)). The GSL Vth distribution between the two processes was compared. When employing *in-situ* boron-doping of SEG instead of boron implantation after SEG, the GSL Vth distribution is improved, as shown in Figure 4. This enhancement is because the boron concentration in the SEG is affected by the hole profile in the case of *ex-situ* boron implantation, but the boron concentration in the *in-situ* boron-doped SEG is not affected. The ion implantation process has straightness by beam energy and boron is doped into the target, so the amount reaching the target surface is determined according to the target size and path. In addition, diffusion occurs by a subsequent activation heating process. In the case of an adjacent hole, the boron is diffused into the nearby CSL, so that the concentration difference from the away hole increases even more. Conversely, in the case of *in-situ* boron-doped SEG, the doping concentration is relatively less affected by the channel hole size and bending degree because doping proceeds by a gas phase diffusion method at a high temperature and low pressure. Furthermore, since deposition is performed at a high temperature, boron diffusion caused by additional heating seems to disappear.

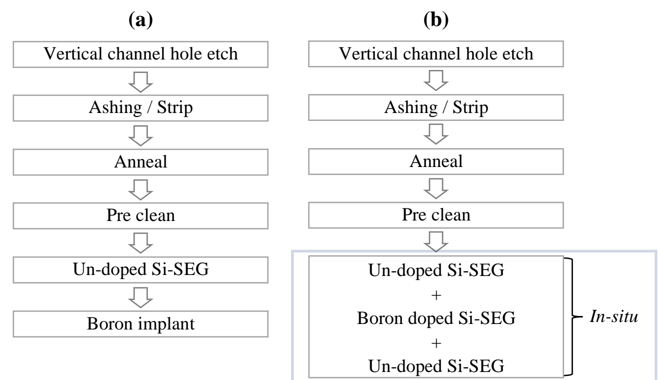


Figure 2. The experimental sequence from vertical channel hole etch to SEG. (a) *Ex-situ* boron implantation (b) *in-situ* b-doped SEG.

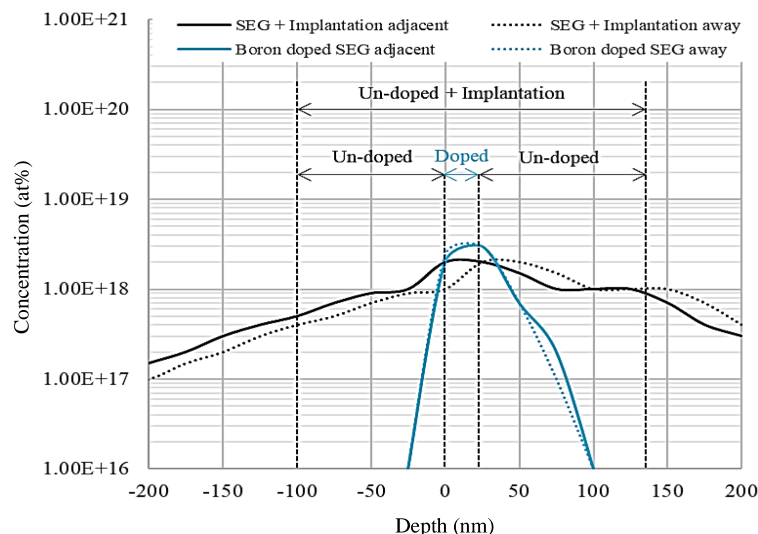


Figure 3. Pattern SIMS Profile. (a) SEG + boron implantation and (b) boron doped SEG.

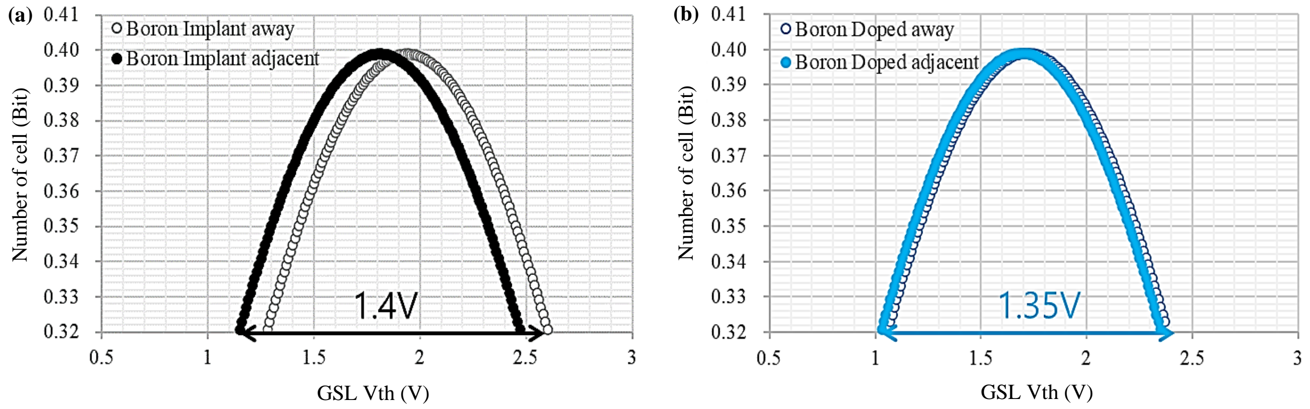


Figure 4. GSL Vth Distribution. (a) GSL of boron implantation and (b) GSL Vth of boron doped SEG.

3.2 Analysis of boron doped SEG process.

Different boron-doping depths and concentrations were studied to find the optimal distribution of SEG height and GSL Vth, with a smaller SEG height variation indicating a more uniform growth rate. The SEG height is defined as the distance from the substrate to the top of the SEG plug, as shown in Figure 5(a). The experimental details are summarized in Table 1.

When boron doped SEG was deposited directly on the sub-silicon layer, the SEG height distribution became poor (Figure 5(b)). This is because the silicon growth rate rapidly increases, caused by an enhanced H-desorption when B atoms are present on the surface. [6] Therefore, the thickness distribution was improved when boron doping SEG was performed after a layer of un-doped SEG was deposited.

The reason for re-depositing un-doped SEG after the boron-doped SEG is that if boron is distributed beyond the vicinity of the GSL transistor, the GSL Vth distribution increases. Therefore, the boron doped SEG area is only desired adjacent to the GSL transistor, following the proper projection range of dopant in implantation. Therefore, this is the reason for forming the triple layer of un-doped SEG/boron-doped SEG/un-doped SEG.

Additionally, we find that the GSL Vth distribution deteriorated when boron doped SEG was formed beyond the GSL region. Consequently, the un-doped/boron-doped/un-doped triple structure is the most optimal scheme for SEG thickness and GSL Vth distribution. Furthermore, the GSL Vth distribution changed according to the boron doping thickness and flow rate, so the optimal concentration could be found through experimental evaluation.

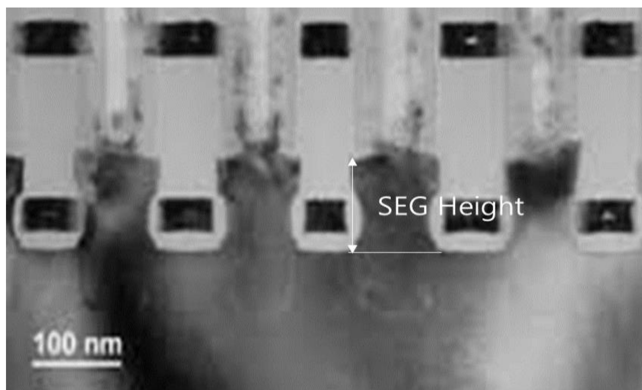
The experimental results confirmed that the higher the boron doped SEG thickness and boron flow rate, the worse the GSL Vth variation. The GSL lower Vth increases as the boron moves to the bottom of the GSL, and the GSL upper Vth increases as the boron moves to the top of the GSL. If the boron flow rate is high, the same phenomenon occurs because diffusion occurs even with the un-doped SEG at the bottom and top. This is because the ratio of depletion width (W_d) is sensitively dependent upon the boron doped SEG thickness and concentration increase, as shown in the following equation [7].

$$V_{th} = V_{FB} + 2\phi_F + \frac{qN_{Trap}W_d}{C_{ox}}$$

The reason why the GSL Vth is more sensitive to these factors is that the bottom of the vertical channel is formed with N-type doping, so it is highly dependent on the boron doping of the SEG.

Table 1. Summary of boron flow rate vs GSL Vth distribution.

Boron Doped Thickness Ratio	Boron Flow Rate (sccm)			
(%)	**0**	**50**	**70**	**90**
0	1.35			
20		1	1.1	1.25
30		1.2		



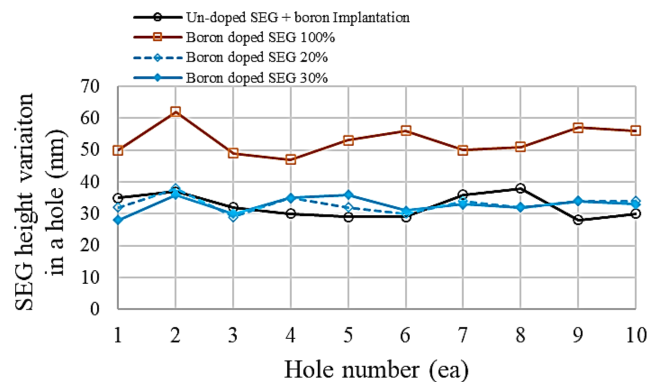


Figure 5. (a) TEM image of SEG height (b) The comparison of un-doped SEG vs. boron doped SEG height variation.

4. Conclusions

In this work, we show that a high-aspect-ratio VCE generates hole profile differences between the adjacent hole and away hole from the CSL, which deteriorates the SEG height uniformity and results in poor GSL Vth distribution. *In-situ* boron doping of triple-layer un-doped/boron-doped/un-doped SEG improves the boron distribution and GSL Vth variation between the adjacent and away holes. Excess of the boron-doped thickness and boron concentration increases the GSL Vth variation. Consequently, suitable boron-doping position and thickness, as well as boron concentration, are critical to providing an appropriate GSL Vth and SEG height variation.

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