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# High temperature storage reliability of Cu pillar flip chip interconnects

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**Abstract**

The Cu pillar flip chip is currently designed and used in the optic communication device that it has exhibited low reliability at high temperature. This paper aims to report the reliability of Cu pillar flip chip assembled on electronics board for a new optoelectronic product subjected to high temperature storage testing. The test was performed at 150°C isothermal condition with the various storage times up to 2000 h. The aged samples were characterized with scanning acoustics microscopy, scanning electron microscopy, and energy dispersive X-ray spectroscopy. Two types of intermetallic compounds (IMCs) were found at beside of the Cu pillar i.e. $Cu_6Sn_5$ and $Cu_3Sn$. The $Cu_3Sn$ layer exhibits a thinner thickness (~0.62 μm at 1000 h) and a slower growth rate (~0.27 μm/1000 h) compared to the $Cu_6Sn_5$ layer (~7.96 μm and ~2.59 μm/1000 h). Cracks were commonly found at the IMC/Cu pillar sidewall interface that initiating at the solder edge on the pillar side with the smaller solder volume, then propagating along IMC/Cu interface. At the top of Cu pillar and substrate pad, which were coated by Ni layer, only $(Cu,Ni)_6Sn_5$ was found. The Ni layer influenced both the IMC type and growth rate. All IMCs exhibited increasing thickness with storage time. These findings provide important insights into the thermal reliability of a fine pitch Cu pillar solder interconnects in advanced electronic packaging.

## 1. Introduction

Nowadays, electronic devices have evolved and trended to a smaller and higher performance with multifunction. Flip chip technology has developed as a leading solution for high-density electronic packaging. This technology enables the integration of multiple functional modules into a single package. Traditionally, the flip chip packages based on solder balls have been widely adopted. However, as package designs move toward extremely fine pitches, the limitations of solder ball technology become increasingly evident. In recent years, Cu pillar bump technology plays an important role in the electronic packaging to have more I/O density, decrease in the spacing between bumps, improve electrical and thermal conductive, increase data transfer speed, thus promoting wider applications of Cu pillar bumps flip chip technology in electronic product with high-density packaging [1,2,3]. Consequently, this technology has been increasingly implemented in next-generation optoelectronic modules, including optical transceivers and laser driver circuits.

However, the reliability of Cu pillar flip chip in optoelectronic product remains a critical concern, especially under mechanical and thermal stress. This concerns strongly relate to the interconnect formed by the solder joint. The miniaturized size of Cu pillars introduces new challenges caused by the coefficient of thermal expansion (CTE) mismatch among Cu pillar, intermetallic compound (IMC) layer and solder, resulting in thermal stresses that can induce creep and fatigue failures in the solder joints [4,5]. In addition, the high temperature condition can lead to the growth of IMC and the formation voids and cracks [6].

In this study, the reliability of Cu pillar flip chip packages assembled on a new optoelectronic product is investigated under high temperature storage test conditions. The Cu pillar flip chip is connected by SnAg solder bump on Cu pillar and SAC305 solder paste on substrate pad. The analysis is performed with scanning acoustic microscope (SAM), optical microscope (OM), scanning electron microscope (SEM), and energy dispersive x-ray spectroscopy (EDS).

## 2. Experimental procedures

Figure 1(a) illustrates a top view schematic of optoelectronic product with assembled five Cu pillar flip chips on substrate that a biggest flip chip is connect with a waveguide laser whereas the other four smaller flip chips are positioned nearby. Figure 1(b) presents the Cu pillar diagram, which shows the structure before soldering of Cu pillar with Ni surface finish and SnAg solder bump on the chip side, and substrate pad with Ni surface finish and SAC305 solder on the board side. The dimensions of this fine-pitch Cu pillars are 0.08 mm in diameter, 0.04 mm in height, and 0.15 mm in pitch.

Figure 2 shows the sample preparation process for the optoelectronic board with Cu pillar flip chip. The chips were initially flipped and placed on the substrate (interconnect structure as shown in Figure 1), followed by the first reflow soldering to establish electrical and mechanical connections between chips and substrate. Subsequently, solder balls

were placed on the bottom side of substrate and were soldered on substrate ball pads by the second reflow. After soldering, an underfill material was applied to completely fill the area beneath each chip in order to enhance the mechanical reliability and thermal performance of the flip chip assembly. Table 1 and Table 2 shows reflow profile implemented to the first and the second reflow soldering, respectively. (In the second reflow profile, shorter reflow time and lower maximum temperature is specified to prevent device damage.)

The reliability test, high-temperature storage (HTS) referring to MIL-STD-883L Method 1005.1 standard [7], was performed to evaluate the effects of isothermal aging on Cu pillar interconnect at 150°C of a constant aging temperature, with a varying duration from 250 h to 2000 h of aging time.

After the high temperature storage test, the samples were first examined by scanning acoustic microscopy (SAM) to detect internal voids or delamination in a non-destructive manner. However, SAM provides limited resolution for distinguishing fine microstructural defects, its results were used primarily for preliminary reliability screening. Subsequently, the samples were prepared by cross-section technique that were polishing down to 0.3 µm. The cross-sectioned samples were characterized by optical microscopy (OM), scanning electron microscopy (SEM) and energy dispersive X-ray spectroscopy (EDS) to investigate microstructure at the interconnect area and to identify the intermetallic compound (IMC) phases. IMC thickness measurements were conducted at 9 sampling points in each analyzed area to investigate the effect of aging time and interfacial material on IMC growth. Figure 3 showed the cross-section plane, optical micrograph, and the three investigated sampling locations that represent in the left, middle, and right area. These cross-section plane and the three sampling locations were selected based on the expectation that a larger electronic component assembled on the board are subjected to a higher residual stress and a higher possibility to failure [8].

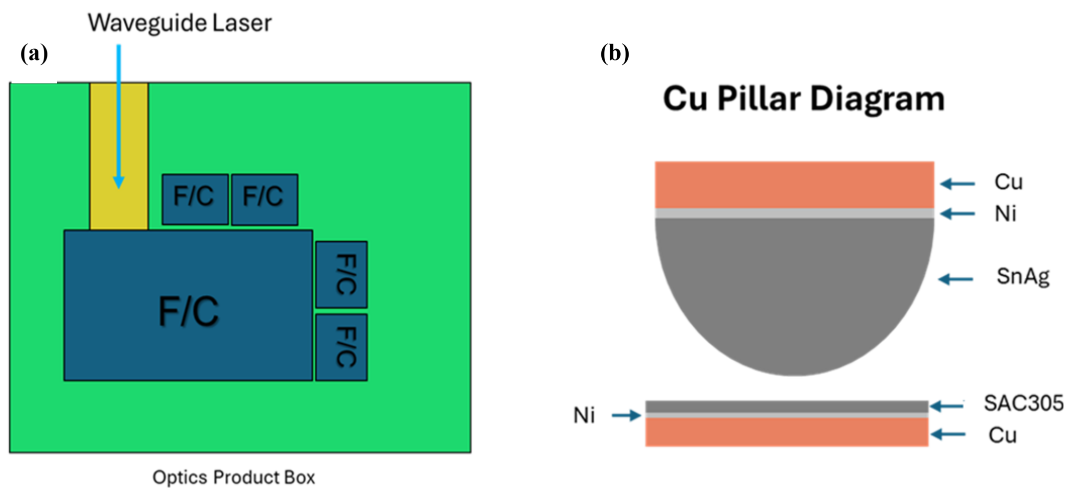


**Figure 1.** (a) Top view schematic of optoelectronic product with assembled Cu pillar flip chip on board (b) structure of Cu pillar and substrate before soldering.

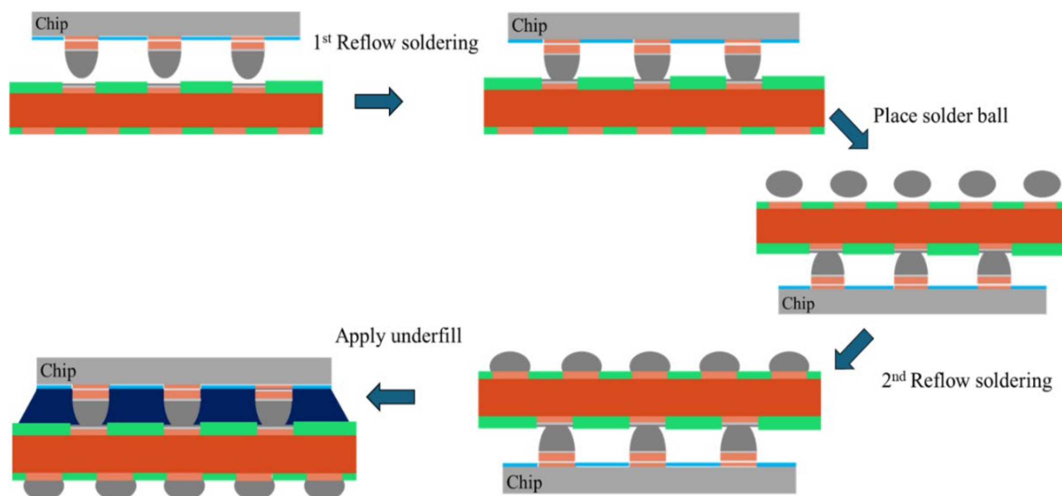


**Figure 2.** Sample preparation process

**Table 1.** Reflow profile implemented to the first reflow soldering.

| Reflow zone | Preheat | Soaking | Reflow (TAL) | Max Temperature |
|---|---|---|---|---|
| Temperature | 130°C | 130°C to 180 °C | 220°C | 255°C to 260 °C |
| Specification | < 4°C·s$^{-1}$ | 50 s to 70 s | 100 s to 110 s | |

**Table 2.** Reflow profile implemented to the second reflow soldering.

| Reflow zone | Preheat | Soaking | Reflow (TAL) | Max Temperature |
|---|---|---|---|---|
| Temperature | 130°C | 130°C to 180 °C | 220°C | 230°C to 240°C |
| Specification | < 4°C·s$^{-1}$ | 60 s to 120 s | 20 s to 70 s | |

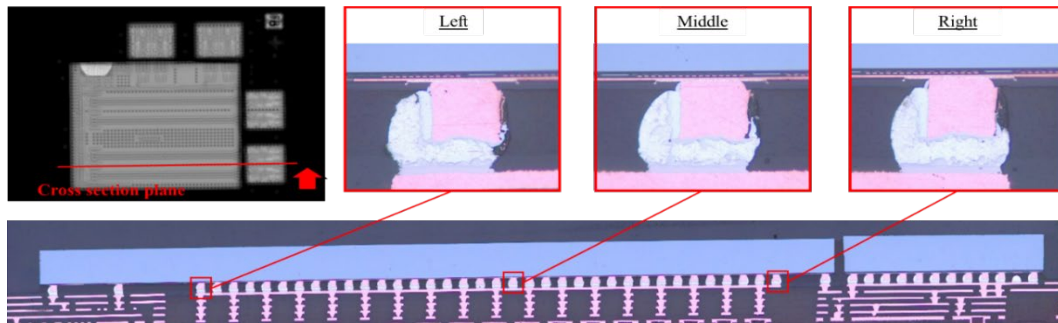


**Figure 3.** Optical micrographs of cross-sectioned sample and sampling investigated location, representing as left, middle, and right.

## 3. Results and discussion

### 3.1 Voids and delamination in Cu pillar solder bump package

Figure 4 shows C-scan acoustic images obtained from the opto-electronic samples after various high-temperature storage durations. This non-destructive imaging technique was used to assess the integrity of the Cu pillar flip chip interconnects, particularly focusing on the solder joints to detect internal voids, cracks, or delamination. The absence of white spots at the Cu pillar and solder bump locations across all aging conditions can imply that the solder joints remained intact and free from void defect throughout the thermal aging. However, these acoustic imaging results are just the preliminary joint reliability detection that still need the confirmation by the other microstructural studies in the subsequent sections.

### 3.2 Microstructure and defects in Cu pillar solder bump interconnects

Figure 5 shows cross section electron micrographs of the interconnects at different sampling locations, obtained from samples with various storage times. Some voids were found in the solder bulk that might generate due to the volume shrinkage during the formation of IMC [5]. The presence of voids can significantly influence the mechanical integrity of solder joints where large voids reduce the load-bearing area, accelerating crack initiation under stress. Most of SEM images reveal cracks at the edge of solder bulk and cracks along the interface between IMC layer and Cu pillar. Both types of cracks are affected from CTE mismatch among the materials (solder, underfill, Cu pillar, and IMC). Cracks at the edge of solder bulk near Cu pillar/IMC layer interface can be caused by CTE differences of solder, IMC, and Cu pillar with the excessive plastic deformation (creep) of solder bump over than IMC and Cu pillar material, incorporating with the thickened IMC layers, leading to high stress concentration and crack initiation [9-11]. The electronmicrographs illustrate that the cracks along the interface between IMC layer and Cu pillar typically occur on the side with a smaller solder volume, and propagate along the IMC layer and Cu pillar interface because the low solder volume is insufficient support the accumulated thermal stress, causing the thermal stress to be directly transferred to the brittle IMC layer.

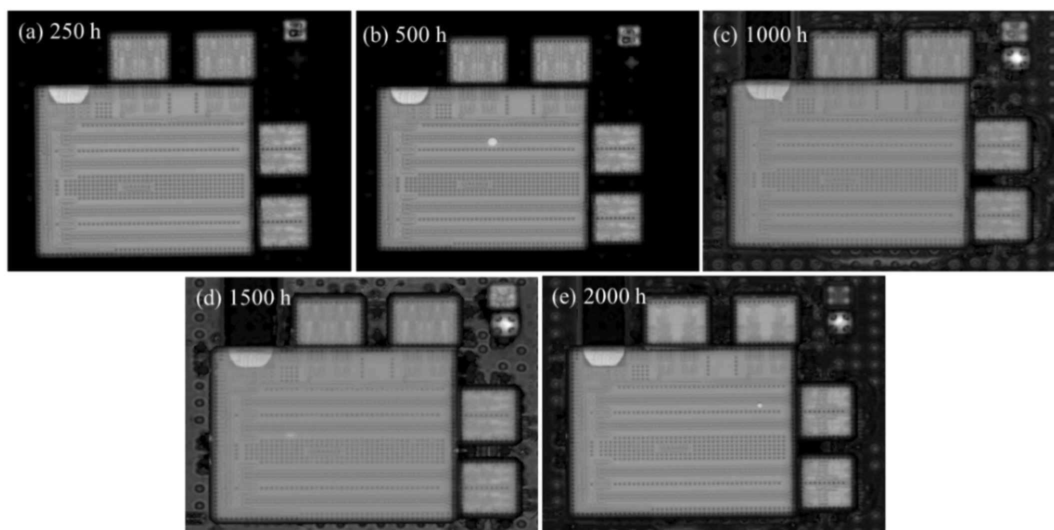


**Figure 4.** Acoustic images obtained from samples with various storage times (a) 250 h, (b) 500 h, (c) 1000 h, (d) 1500 h, and (e) 2000 h.

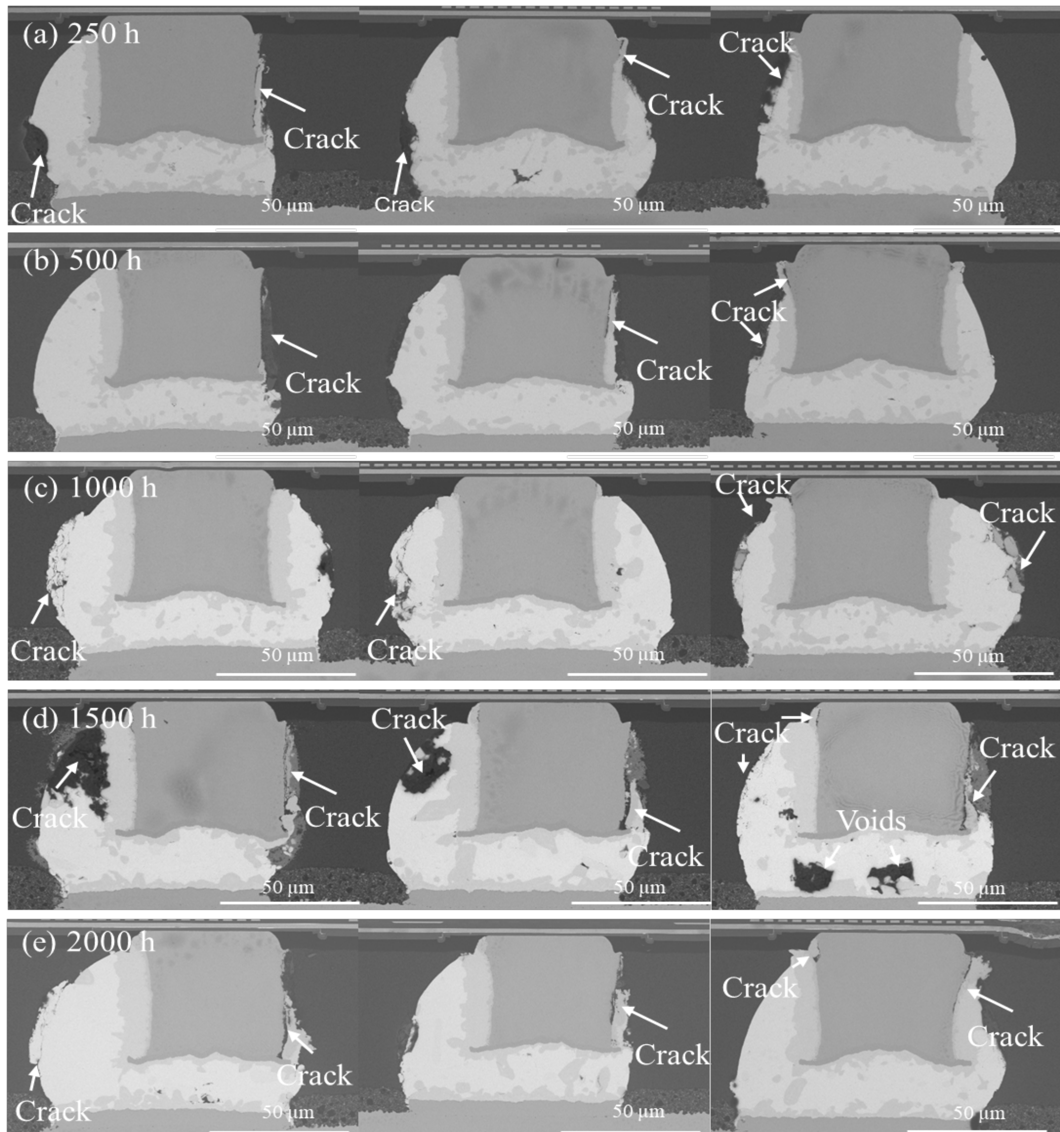


**Figure 5.** Electron micrographs of the sampling interconnects obtained from samples with various storage times (a) 250 h, (b) 500 h, (c) 1000 h, (d) 1500 h, and (e) 2000 h.

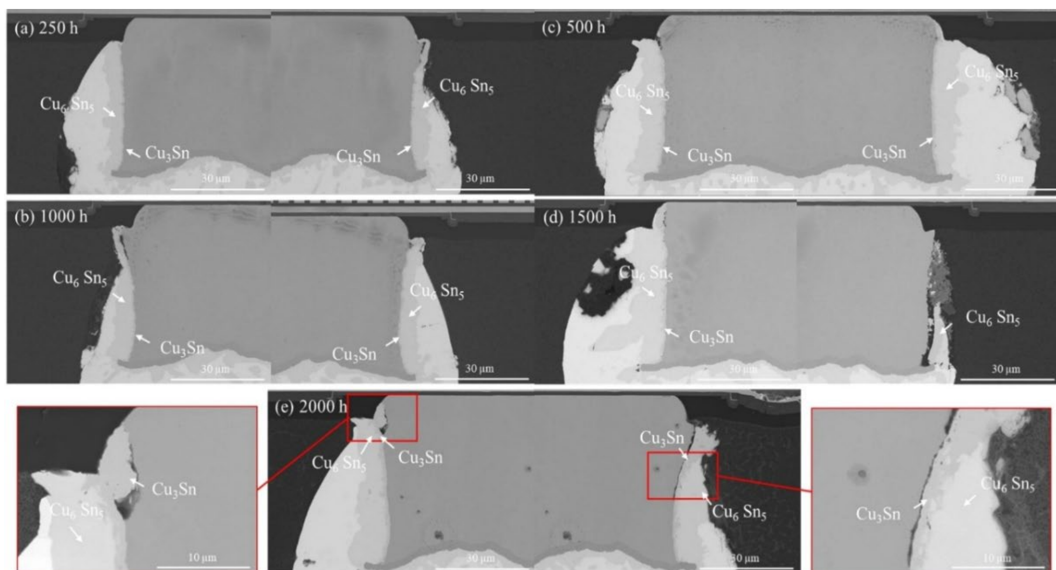


**Figure 6.** IMC phase at beside (left and right) of Cu pillar analyzed on samples with various storage times (a) 250 h (b) 500 h (c) 1000 h (d) 1500 h (e) 2000 h.

### 3.3 IMC phase identified by element analysis

The IMCs formed adjacent to Cu pillars were analyzed by EDS, the two types of IMCs were identified i.e. $Cu_6Sn_5$ and $Cu_3Sn$ as shown in Figure 6. Moreover, the analysis showed that the cracks at side of Cu pillar initiated with the brittle IMC phase of $Cu_3Sn$, as the illustrated in the zoom-in images in Figure 6(e). The top of Cu pillar and substrate Cu pad coated by Ni layer obviously influences to IMC layer that formed a ternary $(Cu,Ni)_6Sn_5$ IMC at the interface, as shown in Figure 7. In addition, $Cu_6Sn_5$ is observed as a dispersed IMC phase in the solder bulk that the distribution and morphology might affect to the overall mechanical properties of the interconnect. The greater $Cu_6Sn_5$ IMC precipitated phase in solder contributed to decreases the mechanical property [12].

### 3.4 IMC Thickness Measurements

Figure 8 presents the box plot illustrating the measured thickness of IMC adjacent to the side of Cu pillar, specifically on $Cu_6Sn_5$ (in red) and $Cu_3Sn$ (in blue), at the various storage times. Both $Cu_6Sn_5$ and $Cu_3Sn$ layer exhibits growth when storage times increase. The mean thickness of both IMC layers increased in correlation with the aging duration. However, the $Cu_3Sn$ layer growth rate is slower than $Cu_6Sn_5$ and remains consistently thinner than the $Cu_6Sn_5$ layer along the testing time. In addition, the thickness of $Cu_6Sn_5$ IMC layer seems to stabilize after approximately 1500 h of storage time, due to the $Cu_3Sn$ and $Cu_6Sn_5$ layer acting as the diffusion barrier between Cu pillar and solder. This behavior represents the evolution of the IMC layers over time, that enhances the understanding about reliability and failure mechanisms of Cu pillar flip chip interconnects under thermal stress.

In Figure 9, the box plots of IMC thickness at the top of Cu pillar and at the substrate pad show that the presence of Ni layer significantly affects to IMC growth behavior. As illustrated in the boxplot, the mean thickness of the $(Cu,Ni)_6Sn_5$ IMC layer increases with prolonged aging, however, its growth rate is slower compared to the $Cu_6Sn_5$ and $Cu_3Sn$ IMC layer formed adjacent to the side of the Cu pillar as reported in Figure 8, due to Ni layer acts as a diffusion barrier, effectively suppressing IMC growth.

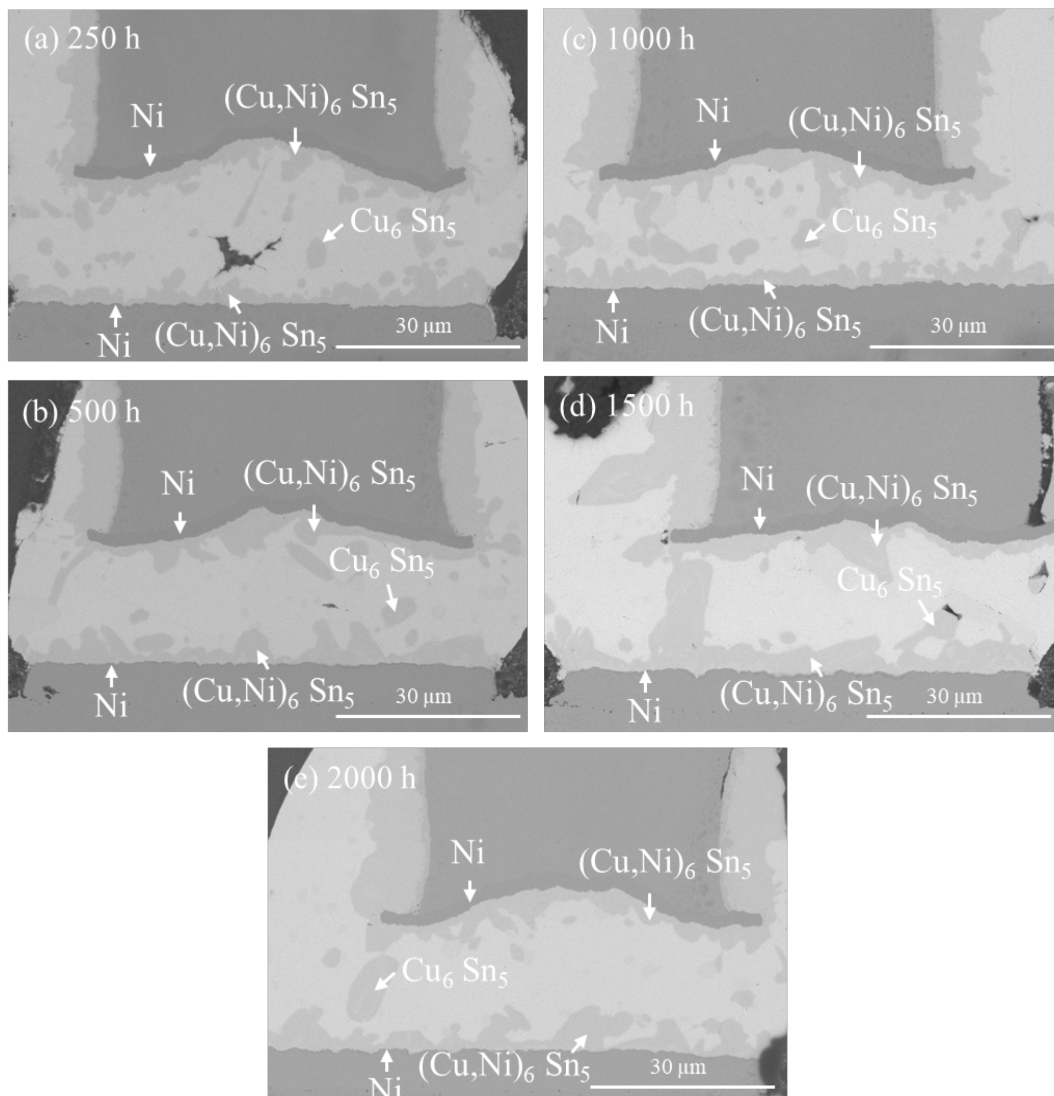


**Figure 7.** IMC phase at top of Cu pillar and substrate Cu pad coated by Ni layer analyzed on samples with various storage times (a) 250 h (b) 500 h (c) 1000 h (d) 1500 h (e) 2000 h.

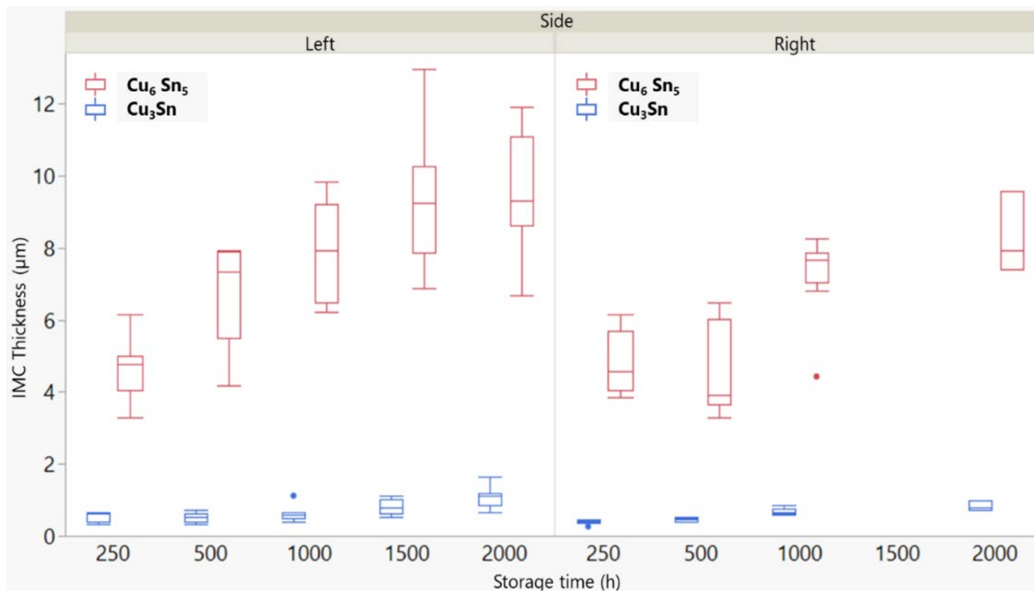


**Figure 8.** Thickness of $Cu_6Sn_5$ (in red) and $Cu_3Sn$ (in blue) IMC layers adjacent to the side Cu pillar measured from samples with various storage times.

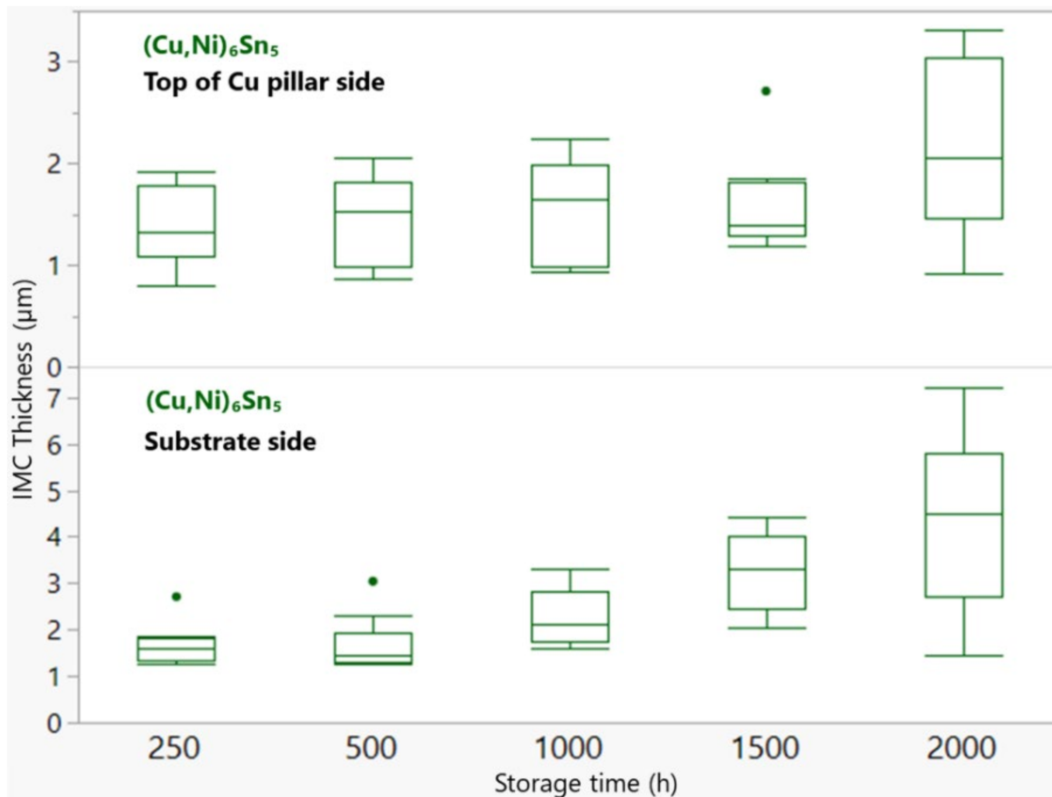


**Figure 9.** The $(Cu,Ni)_6Sn_5$ IMC layer thickness at the top of Cu pillar and substrate side measured from samples with various storage times.

## 4. Conclusions

In this work, the high temperature storage reliability of Cu pillar flip chip solder bump was investigated under and isothermal aging condition of 150°C for up to 2000 h. The main findings can be summarized as follows:

- Cracks are always found at the edges of solder bumps and along the interface between the IMC layer and the Cu pillar.
- The cracks originally started at the edge of the solder bump on the pillar side with the smaller solder volume and subsequently propagated along IMC layer/Cu pillar interface, essentially affecting on a brittle $Cu_3Sn$ layer. To reduce crack initiation, a proper and balance solder volume is needed to reduce local stress concentration, especially near Cu pillar side.
- Three types of IMCs were identified in this Cu pillar package i.e. $Cu_6Sn_5$, $Cu_3Sn$, and $(Cu,Ni)_6Sn_5$. All IMC layers thickened by

the longer storage times, however, $Cu_6Sn_5$ thickness demonstrates a trend toward saturation after a prolonged high temperature storage time, reflecting characteristics of IMC growth behavior over time.

- The $Cu_3Sn$ IMC layer is typically thinner throughout the test and exhibited a slower growth rate compared to $Cu_6Sn_5$.
- The $(Cu,Ni)_6Sn_5$ IMC layer is only found at the interface between the solder bulk and the Ni layer, where the presence of Ni behaved as a diffusion barrier, promoting a slower IMC growth. Therefore, Ni layer can be used to suppress excessive IMC growth and enhance interfacial stability during long time under high temperature storage.

This study provides a comprehensive understanding of the IMC evolution and failure mechanisms of Cu pillar flip-chip interconnects under high temperature storage test. The experimental findings can serve as useful guidelines for improving the long-term reliability of Cu pillar interconnects in next-generation optoelectronic products and high-performance electronic packaging applications.

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## References

[1] K. Pongvittayapanu, A. Srisrual, and K. Fakpan, "Effect of thermal cycling and vibration on cracking in Sn-3.0Ag-0.5Cu solder bump," *Materials Today: Proceedings*, vol. 52, pp. 2372-2376, 2022.

[2] J. Li, Y. Zhang, H. Zhang, Z. Chen, C. Zhou, X. Liu, and W. Zhu, "The thermal cycling reliability of copper pillar solder bump in flip chip via thermal compression bonding," *Microelectronics Reliability*, vol. 104, p. 113543, 2020.

[3] R. Alberti, R. Enrici Vaion, A. Mervic, and S. Testa, "Metal fatigue in copper pillar Flip Chip BGA: A refined acceleration model for the aluminium pad cracking failure mechanism," *Microelectronics Reliability*, vol. 55, pp. 1838–1842, 2015.

[4] Q.-S. Zhu, Z.-F. Ding, X.-F. Wei, J.-dong Guo, and X.-J. Wang, "Effect of leveler on performance and reliability of copper pillar bumps in wafer electroplating under large current density," *Microelectronics Reliability*, vol. 146, p. 115030, 2023.

[5] S. Wang, J. Feng, W. Wang, P. Wu, J. Wen, D. Yang, Y. Huang, R. Tian, S. Wang, and Y. Tian, "Isothermal aging and electromigration reliability of Cu pillar bumps interconnections in advanced packages monitored by in-situ dynamic resistance testing," *Journal of Materials Research and Technology*, vol. 32, pp. 937-954, 2024.

[6] X. Jing, W. Sun, L. Cao, P. He, and S. Zhang, "Phase transformation, microstructural evolution and mechanical degradation of SnAg2.4/Cu solder joints at 160°C high-temperature storage test," *Materials Characterization*, vol. 221, p. 114802, 2025.

[7] U. S. Department of defense, "MIL-STD-883L 1005.11," in *Test Method Standard Environment Test Method for Microcircuits*, 2019, pp. 27-36.

[8] C. F. Coombs, Jr., *Printed circuits handbook*. New York: McGraw-Hill, 2008.

[9] J. Libres, and J. C. Arroyo, "Investigation of bump crack and deformation on Pb-free flip chip packages," *Electronic Components and Technology Conference*, pp. 1536-1540, 2010.

[10] D. Kim, J. Park, J. Jang, H. Yang, K. Kim, and C. Oh, "Underfill material property dependence of lifetime and mechanical behavior of BGA package: EBSD and FEM investigations," *Microelectronics Reliability*, vol. 150, p. 115113, 2023.

[11] N. Ismail, W. Y. Wan Yusoff, A. Amat, N. A. A. Manaf, and N. Ahmad, "A review of extreme condition effects on solder joint reliability: Understanding failure mechanisms," *Defence Technology*, vol. 41, pp. 134-158, 2024.

[12] P. Jattakul, T. Madsa, P. Sunasuan, and N. Mookam, "Influence of cooling conditions on microstructure and mechanical property of Sn-0.3Ag-0.7Cu lead-free solder," *Journal of Metals, Materials and Minerals*, vol. 31, no. 2, pp. 129-136, 2021.